張毓珍

Yu-Chen Chang

Contact

+886929593707

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2000.07.06

Skills

Programming Languages:
C++ / MATLAB / Verilog

CAD-Tools:
HSPICE / Virtuoso / Laker

Language Proficiency:

Mandarin: Native
English: IELTS 7.0 / TOEIC 890

Internship

2022 TSMC summer intern

(Jul. 2022 - Aug. 2022)

Scholarship

College of Semiconductor Research Scholarship

(Sep. 2022 - Sep. 2024)

Micron Scholarship

(Sep. 2022 - Sep. 2023)

Project

8K-bit SRAM Macro

(Embedded Memory Circuit Design, A+)

512-bit ROM Macro

(Introduction to Integrated Circuit Design, A-)

BIST Design for SRAM

(VLSI Testing, A+)

A Fully-Differential Two-Stage Op-Amp

(Analog Circuit Design, A-)

Single Slope ADC

(Analog Circuit Design)

Lab

Professor: Meng - Fan Chang Ph.D

Research Field:

Compute-in-Memory (CIM) for AI chips

Memory Integrated Circuit

Education

UC Berkeley EECS Visiting specialist

(Jan. 2025 – Aug. 2025)

National Tsing Hua University

Master in College of Semiconductor Research

Final defense completed in Oct. 2024

(Sep. 2022 – Aug. 2025)

National Tsing Hua University

Bachelor of Science

1st program – Biomedical Engineering and Environmental Sciences

2ed program – Electrical Engineering

(Sep. 2018 – Jun. 2022)

IC Tape-out Experience

2023Q2 TSMC-NTHU JDP 22nm ReRAM-CIM

- New idea of ReRAM-CIM for better energy efficiency
- ReRAM BL Clamping & Writing Circuit Design

2024Q2 TSMC-NTHU JDP 22nm ReRAM-SRAM-Fusion-CIM Processor

- New idea of SRAM-CIM Local Computing Cell
- SRAM-CIM Macro design

Publication & Patents

2024 IEEE International Solid-State Circuits Conference (ISSCC) pp. 580-582, Feb. 2024

"A 22nm 16Mb Floating-Point ReRAM Compute-in-Memory Macro with 31.2 TFLOPS/W for AI Edge Devices"

2024 IEEE Journal of Solid-State Circuits (JSSC)

"A 22nm Floating-Point ReRAM Compute-in-Memory Macro Using Residue-Shared ADC for AI Edge Device"

Two US patents Pending